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10/607,081	06/25/2003	John W. Horigan	42P16970	6540

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
HOLTON, STEVEN E	
ART UNIT	**PAPER NUMBER**
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/607,081	HORIGAN, JOHN W.	
	Examiner	Art Unit	
	Steven E. Holton	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-8,10-14 and 16-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-8,10-14 and 16-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is made in response to applicant's amendment filed on 12/11/2006. Claims 1,2,4-8, 10-14, and 16-20 are currently pending in the application. An action follows below:

Response to Arguments

2. Applicant's arguments filed 12/11/2006 have been fully considered but they are not persuasive.

Regarding claim 1, the Examiner respectfully disagrees with the arguments that Chao fails to teach using a counter for counting clock signals and transmitting a feedback signal to a clock source to alter the clock source. In this case the Examiner is considering the Phase Detector (Fig. 7A, element 150) and the Filter (Fig. 7A, element 160) to be a single unit that is analogous to the counter used in the current application and shown in Fig. 5 and further described in paragraph 29. The counter defined by the applicant is a circuit that is connected to two different PLL circuits (Fig. 5, elements 501 and 505) and is used "to count the clock edges of the clock signal out of each PLL". Further, the counter then determines when there is a difference between a number of clock edges from each source over a period of time, and finally "sends a feedback signal to the PLL 505 to cause the PLL 505 to adjust the center frequency of the SSC clock signal." The circuit of Chao shown in Figs. 7A and 7B performs the same function as the counter of the application. The circuit shown by Chao takes in inputs from two clock signals (signals wr and rd); it counts the number of clock edges of each of the

signals (Fig. 7b, elements 171 and 172); then determines when there is a difference between the number of clock edges from each source (Fig. 7b, elements 174 and 175); and finally outputs a feedback signal directly to the PLL clock signal source to manipulate the clock frequency (Fig. 7a, element 160 connects to element 180 to transmit a feedback signal. Chao further describes this in col. 11, line 4 – col. 12, line 12. The combination of elements 150 and 160 of Chao perform the same function as the counter element disclosed by the Applicant; therefore, the Examiner considers these elements to be the 'counter' discussed in claims 1. Regarding the clock sources, Fig. 7a, element 180 of Chao is the source of the rd clock signal of Chao and some other circuit element is used to produce the wr clock signal (element 82) that is input into counter element 171. The current application further shows that it is a matter of design choice to provide two clock sources (Fig. 4a, elements 410 and 420) or a single clock source that is later modified (Fig. 4b, element 410). At the time of invention it would be obvious to one skilled in the art that Chao is using two different clock sources to generate the rd and wr signals because the source of the rd clock signal (Fig. 7a, element 180) is not used to generate the wr clock signal.

On the arguments regarding independent claims 2, 8, and 14, the Examiner respectfully disagrees with the Applicant's arguments that Beale fails to transmit a signal when the content of a buffer reaches a predetermined threshold value. The buffer described by the Applicant in Fig. 4a, element 404 and similar performs the functions of receiving data from an input, transmitting data away through an output and uses two clock signals to control the input and output transmissions respectively.

Further, the buffer then provides a signal indicating when the content of a buffer reaches a predetermined threshold value. The system of Beale shown in Fig. 3, comprises a data buffer and a data buffer counter that determines the size of the content of the buffer (col. 10, lines 20-42). Finally, when the amount of information in the buffer reaches a predetermined threshold value, a signal is transmitted to the second clock source to change the clock frequency to keep the buffer from overflowing or underflowing (col. 10, lines 43-64). The Examiner then logically groups the elements of Beale that perform these calculations (Fig. 3, elements, 32, 124, 120, and 100) and reads these components to be analogous and equivalent to the 'buffer' described in claims 2, 8, and 14.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4-7, 10-13, and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants Admitted Prior Art (paragraphs 4-6 of the disclosure), hereinafter AAPA, in view of Chao et al. (USPN: 5007070), hereinafter Chao.

Regarding claim 1, AAPA discloses a prior method of generating a pixel stream from a non-SSC clock (paragraph 5, lines 1-2) and forwarding a second clock signal and the first pixel stream to a buffer to translate the first pixel stream based on the

second clock signal (paragraph 5, lines 2-4). The Examiner notes that the AAPA does not expressly state if the clocks come from one or two sources, the use of two sources would be obvious to one skilled in the art. However, AAPA does not expressly disclose providing a feedback to the second source to cause the second source to adjust the center frequency of the second clock signal to match the average frequency of the first clock signal with the average frequency of the second clock signal.

Chao discloses a feedback system to correct differences in frequency between two clock sources (col. 3, lines 3-11). The two clock sources (Fig. 7a, elements wr and rd) being an input clock coupled to an incoming data stream and the output clock source (Fig. 7A, element 180) for reading data out of a buffer. The frequency of the output clock source is changed depending on the difference between the measured clock pulses (Fig. 7A, elements 150 and 160; col. 11, line 30 – col. 12, line 12).

At the time of invention, it would have been obvious to one skilled in the art to modify the teachings of AAPA and Chao to produce a clock system with feedback based on the difference of counts of two clock pulses to correct the frequency of the second clock signal. The motivation for modifying the teachings would be to protect the buffer used in the AAPA from overflow or underflow conditions using a counting and clock frequency changing system as described in Chao. Thus, it would have been obvious to one skilled in the art that the method of counting clock pulses and using the difference between clock pulses to alter clock frequencies to match described by Chao could be used in a graphics system as described by AAPA. The combination of the two would produce a method as described in claim 1.

Regarding claim 4, Chao discloses using a voltage controlled oscillator (Fig. 7A, element 180, described in col. 11, lines 4-18 as element 18). The examiner notes that the voltage controlled oscillator output connected as feedback to the comparison circuit to alter the frequency of the oscillator is a phase locked loop.

Regarding claim 5, AAPA discloses using a non-spread spectrum modulation clock signal (paragraph 5, lines 1-2) and a spread spectrum modulation clock signal (paragraph 5, lines 2-3).

Regarding claim 6, AAPA discloses sending the pixel stream associated with the non-spread spectrum [first pixel stream] to a cathode ray tube display (paragraph 4, lines 6-8) and a pixel stream associated with the spread spectrum clock signal to a liquid crystal display panel (paragraph 4, lines 3-4).

Regarding claim 7, the Examiner notes that this is an apparatus to be operated using the associated method of claim 1. Although there is no provided figure of a display system that would operate as described by AAPA, the Examiner states that the system would inherently possess a first and second circuitry to produce first and second clock signals; a display pipe to generate a first pixel stream based on the first clock signal; and a buffer coupled to the display pipe to receive the first pixel stream and the second clock signal to transform the first pixel stream into a second pixel stream on the second clock signal. The Examiner notes that no specific mention of a display pipe is made in the AAPA, but there would inherently be some device to produce the pixel stream and such a device could be a display pipe, which is known in the art. AAPA does not expressly disclose the second circuitry being coupled to the buffer to receive a

feedback, to adjust the center frequency of the second clock signal and a counter circuit used to produce the feedback signal.

Chao discloses, "a second circuitry coupled to the buffer to generate the second clock signal and to receive feedback to adjust the center frequency of the second clock signal (Fig. 5, element 80 is coupled to element 68, the buffer)". The voltage controlled oscillator (Fig. 7A, element 180 (described as element 18 in the disclosure)) produces the clock signal, rd and receives feedback from the phase detector and filter circuits working in combination (Fig. 7a, elements 150 and 160). The phase detector and filter described by Chao can be equated to the counter described in the claims. The phase detector counts the clock edges and calculates any difference between the clock edges from the first and second sources and produces a signal (up or down) from the decision circuit (Fig. 7b, element 175) based on the difference. The up and down signals are then transmitted to the filter (Fig. 7A, element 160) where the up and down signals are further converted into a single feedback signal that is transmitted to the second clock source (col. 11, line 19 – col. 12, line 12). The feedback signal is then transmitted directly to the clock source (Fig. 7A, element 180).

At the time of invention, it would have been obvious to one skilled in the art to combine the teachings of AAPA and Chao to produce a clock system with feedback based on the difference of counts of two clock pulses to correct the frequency of the second clock signal. The motivation for doing so would have been a matter of design choice. Both the AAPA and Chao provide methods synchronizing multiple clock signals so data are transmitted and buffers holding the data are kept from overflow and

underflow conditions. Thus, it would have been obvious to one skilled in the art that the method of counting clock pulses and using the difference between clock pulses to alter clock frequencies to match described by Chao could be used in a graphics system as described by AAPA. The combination of the two would produce a method as described in claim 7.

Regarding claim 10, Chao discloses using a voltage controlled oscillator (Fig. 7A, element 180, described in col. 11, lines 4-18 as element 18). The examiner notes that the voltage controlled oscillator output connected as feedback to the comparison circuit to alter the frequency of the oscillator is a phase locked loop.

Regarding claim 11, AAPA discloses using a non-spread spectrum modulation clock signal (paragraph 5, lines 1-2) and a spread spectrum modulation clock signal (paragraph 5, lines 2-3).

Regarding claim 12, AAPA discloses sending the pixel stream associated with the non-spread spectrum [first pixel stream] to a cathode ray tube display (paragraph 4, lines 6-8) and a pixel stream associated with the spread spectrum clock signal to a liquid crystal display panel (paragraph 4, lines 3-4).

Regarding claim 13, the Examiner notes that the claim is drawn to a system comprising the device of claim 7 coupled to dynamic random access memory. Therefore, the arguments of claim 7 can be applied to the similar components of claim 13. Regarding the dynamic random access memory, the Examiner states that in a computer system which is what the graphics apparatus of claim 7 would be used in dynamic random access memory (DRAM) would be an inherent and obvious part of the

computer system. DRAM is conventionally used to store program and graphics information in an operating computer system and having it coupled to the graphics controller of claim 7 would be an obvious choice for one skilled in the art.

Thus, the addition of DRAM to the device of claim 7 would have been obvious to one skilled in the art to provide storage for graphics information that would be used by the apparatus of claim 7 to produce pixel streams and other operating information for the computer system.

Regarding claim 16, Chao discloses using a voltage controlled oscillator (Fig. 7A, element 180, described in col. 11, lines 4-18 as element 18). The examiner notes that the voltage controlled oscillator output connected as feedback to the comparison circuit to alter the frequency of the oscillator is a phase locked loop.

Regarding claim 17, AAPA discloses using a non-spread spectrum modulation clock signal (paragraph 5, lines 1-2) and a spread spectrum modulation clock signal (paragraph 5, lines 2-3).

Regarding claim 18, AAPA discloses sending the pixel stream associated with the spread spectrum clock signal [second pixel stream] to a liquid crystal display panel (paragraph 4, lines 3-4).

Regarding claim 19, AAPA discloses sending the pixel stream associated with the non-spread spectrum [first pixel stream] to a cathode ray tube display (paragraph 4, lines 6-8).

Regarding claim 20, the Examiner notes that the graphics memory controller hub is used within a computer system. As such, it would be obvious to one skilled in the art

that the hub would be coupled to a processor that is part of the external computer system. The external processor would be in charge of the computer functions and programs running on the computer.

4. Claims 2, 8 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (paragraphs 4-6 of the disclosure), hereinafter AAPA, in view of Beale et al. (USPN: 5790615), hereinafter Beale.

Regarding claims 2 and 8, the Examiner notes these claims are drawn to a method of operation and associated apparatus. Further the arguments provided were previously used for claims with these limitations in the previous Office Action dated 10/14/2005. The arguments for claim 2 are restated here. AAPA discloses a prior method of generating a pixel stream from a non-SSC clock (paragraph 5, lines 1-2) and forwarding a second clock signal and the first pixel stream to a buffer to translate the first pixel stream based on the second clock signal (paragraph 5, lines 2-4). The Examiner notes that the AAPA does not expressly state if the clocks come from one or two sources, the use of two sources would be obvious to one skilled in the art. However, AAPA does not expressly disclose providing a feedback to the second source to cause the second source to adjust the center frequency of the second clock signal to match the average frequency of the first clock signal with the average frequency of the second clock signal.

Beale discloses a feedback system with two clock signals from different sources (Fig. 3, elements 102 and 104, CLK1 and CLK2) and a data buffer (Fig. 3, element 32).

The feedback system works so that that based on a count of the amount of data within the buffer (Fig. 3, element 120) the second clock signal is altered to match the average frequency of the first clock signal (col. 8, lines 28-35 (mention of matching average rate (frequency)); col. 9 line 58- col. 10, line 64 (detailed discussion of feedback system)). Beale further discloses "sending a signal from the buffer to the second source when the content of the buffer reaches a predetermined threshold value (col. 10, lines 28-42)."

At the time of invention it would have been obvious for one skilled in the art to modify a standard twin mode pixel stream system of AAPA with a system to protect a data buffer from overflow and underflow conditions as used by Beale. The motivation for doing so would have been to protect the data buffer used in the AAPA from overflow and underflow conditions by changing the output clock frequencies (Beale, col. 4, line 66 – col. 4, line 3; Abstract, lines 8-12). Thus, it would have been obvious to combine AAPA and Beale to produce a method of operating a device as specified in claims 2 and 8.

Regarding claim 14, the Examiner notes that the only difference between claims 8 and 14 is the addition of DRAM to be used as a memory with the device as specified in claim 8. As stated in the previous rejection, DRAM is well-known in the art for use in computer systems and it would be obvious to one skilled in the art that DRAM could be combined with the graphic memory controller within a computer system. The Examiner notes that references regarding DRAM were provided with the office action dated 4/19/2006.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven E. Holton whose telephone number is (571) 272-7903. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven E. Holton
Division 2629
March 2, 2007

AMR A. AWAD
SUPERVISORY PATENT EXAMINER